Rejection Under 35 U.S.C. § 102 and/or 103

To the extent any art rejection continues to be applied against claims 6-13 or may be applied against new claims 14 or 15, reconsideration is respectfully requested.

Fukumoto et al. (5,786,616) is directed to a SOI type semiconductor integrated circuit with a protective circuit, which protects against surges between a signal-input terminal and power supply terminal to obtain an improved electrostatic withstand ability. When a surge is applied to the signal-input terminal, a parasitic diode composed by the resistor diffusion region and silicon substrate, exhibits avalanche breakdown, and the surge voltage bypasses the device.

Applicant's present application provides improved switching speeds and memory access times, for example, in devices that include an SOI transistor. In particular, the present application, in a preferred embodiment, is directed to discharging any accumulated potential or charge on the body, i.e., between the source and drain regions of an SOI device. This is accomplished, in part, by generating a pulse that, prior to a first access attempt, enables a body (amended claims 6, 9, 11 and new claims 14, 15) of the SOI transistor to be connected to a lower potential, e.g., ground potential.

Fukumoto et al. do not teach, disclose or suggest "using the pulse discharge circuit to discharge any accumulated potential on a body of the...SOI device...", as recited in amended independent claim 6.

With respect to amended independent claim 9, Fukumoto et al. do not teach, disclose or suggest "selectively grounding the body of at least one of the plurality of SOI devices to dissipate an electric charge accumulated in the body of the at least one of the plurality of SOI devices".

Similar distinctions hold with respect to amended independent claim 11 and to new claims 14 and 15.

Thus, Applicant believes that any art rejection is overcome, without the introduction of new matter.

Accordingly, entry of this Amendment, reconsideration of claims 6-13, consideration of claims 14 and 15, and passage to issue are requested.

Respectfully submitted,

Roy Childs Flaker, et al.

By: 5-13-02

Joseph P. Abate
Registration No. 30,238
Telephone: (845) 894-4633

JPA/rmm

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The following show changes made to page 13, lines 3-26 and page 14, lines 1-13.

When segment driver 450 is activated, the active global word line will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450. The control (CTL) or segment signal is used to select one of the memory subarrays or segments for reading or writing. In circuit 500, CTL is also supplied as an input signal to pulse discharge circuit 310. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by connecting select line 460 to ground. When all three of the input signals to segment driver 450 are active, select line 460 is used to discharge the accumulated charge on the SOI transistors. This time, instead of discharging through segment driver 450 as shown in FIG. 4, the accumulated charge is dissipated through a pull-down transistor in inverter 624 which is located in pulse discharge circuit 310. This is accomplished as follows. In normal operation, to select a given memory subarray, the CTL signal for that subarray transitions from low to high.

This CTL signal is also supplied to pulse discharge circuit 310 as an input signal. After a brief propagation delay through a delay element (invertors or other circuit device), circuit node 621 will transition from high to low. Circuit node 622 will generate a negative pulse and, after passing through an inverter, becomes a positive pulse at node 623. The positive signal or pulse applied to transistor 625 activates transistor 625 which, in turn, provides a path for discharging the word line drivers of memory circuit 500 through inverter 624. The pulse discharge signal generated by pulse generator [520] 510 is the output signal from the pulse discharge circuit and, in a preferred embodiment of the present invention, is supplied to the memory subarray just prior to the selection of the subarray for access. This means that the charge accumulated on the bodies of the SOI transistors has already been discharged when the request to access the subarray is received. By removing the charge before the first access occurs, the access time to the subarray is greatly enhanced. While it is possible to provide a discharge pulse prior to every access, this is not necessary. Once the initial accumulation of charge has been dissipated, as long as subsequent accesses are to the same subarray, there will not be very much charge accumulated in the subarray. By discharging the subarray prior to the first access only, the additional power requirements necessary to implement the invention are minimal. [Once the control signal has selected a given segment, the control signal remains high and no transition of control signal is]

In the Claims

Please amend claims 6, 9 and 11 and add new claims 14 and 15.

6. (Amended) In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device;

using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device.

9. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of: [selecting]

selectively grounding the body of at least one of the plurality of SOI devices to dissipate an electric [potential] charge accumulated in the body of the at least one of the plurality of SOI devices.

11. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising [the step of]:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse

generator connected to the circuit;

using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices [by supplying] to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator [to the body of the at least one of the plurality of the SOI devices at a pre-determined time].

14. (New) A method for discharging accumulated charge from a body of an SOI device and accessing the SOI device, comprising:

generating a pulse;

using the generated pulse to provide a conductive path from the body of the SOI device to a reference point having a lower potential than the accumulated charge;

discharging the accumulated charge from the body of the SOI device to the reference point;

providing a control signal which enables access to the SOI device; and

reading an output of the SOI device,

wherein said steps of generating a pulse and discharging the accumulated charge occur prior to said step of reading an output of the SOI device.

15. (New) A method for reducing memory access time for a memory array which

includes at least one SOI device, the method comprising:

activating a memory segment driver;

selecting a memory segment in the memory array;

generating a pulse in response to said selecting a memory segment;

connecting a select line to a ground potential in response to the generated pulse;

discharging any accumulated charge from a body of the at least one SOI device to the ground potential; and

accessing the selected memory segment after said discharging step.